

FIG. 1a
(PRIOR ART)

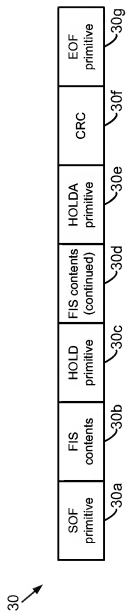


FIG. 1b
(PRIOR ART)

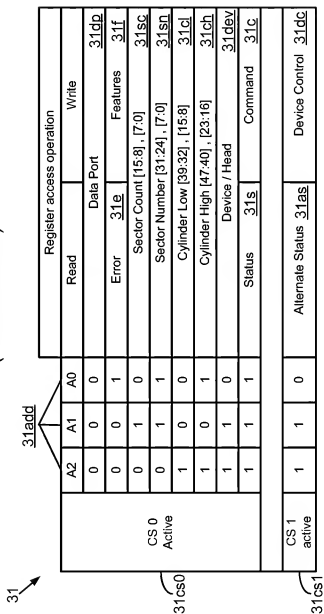


FIG. 1c
(PRIOR ART)

0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)
1	Dev / Head	Cyl High				Cyl Low	Sector Number
2	Features (exp)	Cyl High (exp)				Cyl Low (exp)	Sector Num (exp)
3	Control	Reserved (0)				Sector Count (exp)	Sector Count
4	Reserved (0)	Reserved (0)				Reserved (0)	Reserved (0)

40(i)

FIG. 1d(i) Register FIS Host to Device
(PRIOR ART)

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (39h)
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40(iii)

FIG. 1d(iii) DMA Activate FIS, Device to Host
(PRIOR ART)

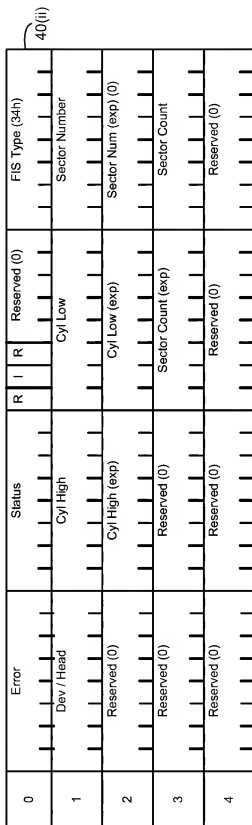


FIG. 1d(ii) Register FIS Device to Host
(PRIOR ART)



FIG. 1d(v) Set Device Bits FIS
(PRIOR ART)

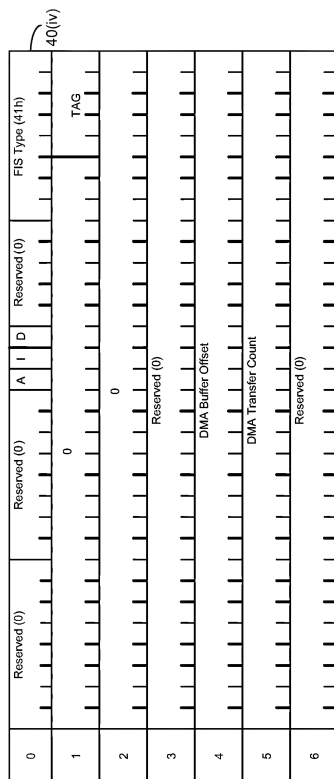


FIG. 1d(iv) DMA Setup FIS
(PRIOR ART)

0	Error	Status			R	I	D	Reserved (0)	FIS Type (5Fh)		
1	Dev / Head	Cyl High			Cyl Low			Sector Number			
2	Reserved (0)	Cyl High (exp)			Cyl Low (exp)			Sector Number (exp) (0)			
3	E_Status	Reserved (0)			Sector Count (exp)			Sector Count			
4	Reserved (0)			Transfer Count							

FIG. 1d (vi) PIO Setup FIS
(PRIOR ART)

0	Reserved (0)	Reserved (0)	R	R	Reserved (0)	FIS Type (46h)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)					
...						
n						

FIG. 1d(vii) Data FIS
(PRIOR ART)

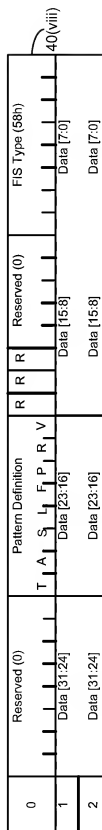


FIG. 1d (viii) BIST Activate FIS
(PRIOR ART)

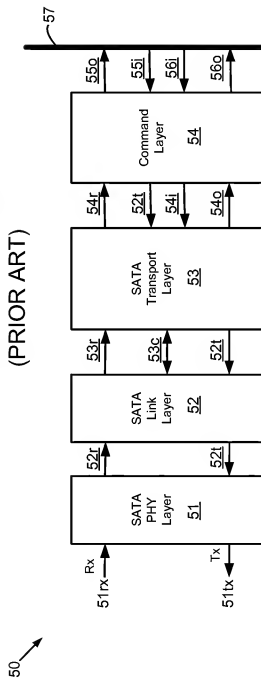


FIG. 2a
(PRIOR ART)

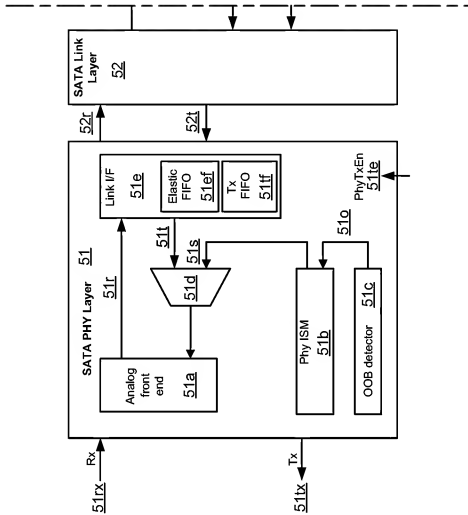


FIG. 2b(i)
(PRIOR ART)

Fig. 2b(i)	Fig. 2b(ii)
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Key To
FIG. 2b

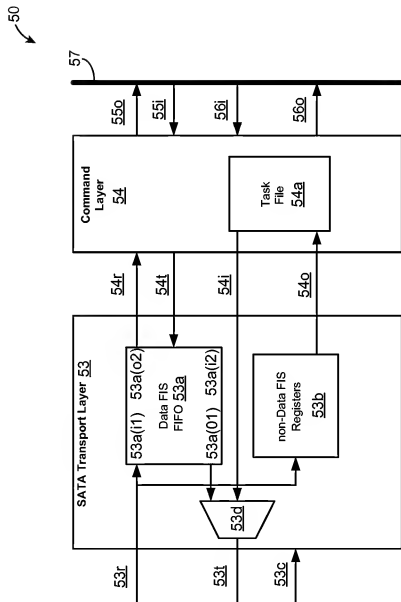


FIG. 2b(ii)
(PRIOR ART)

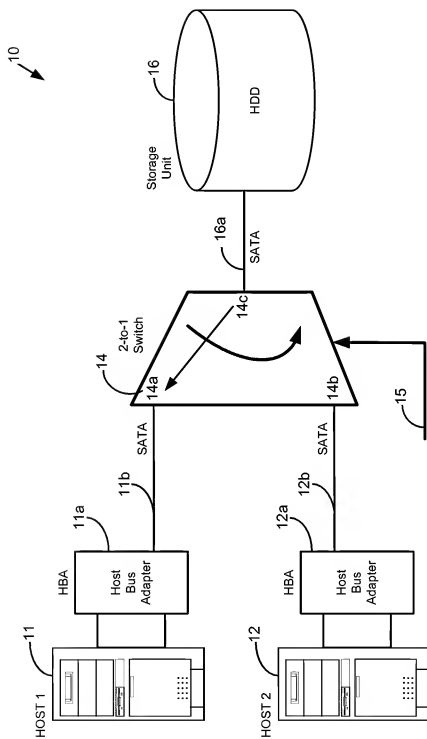
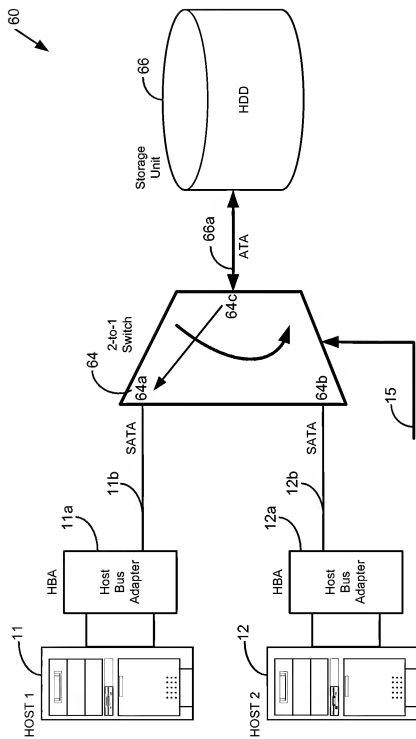


FIG. 3a
(PRIOR ART)

FIG. 3b
(PRIOR ART)

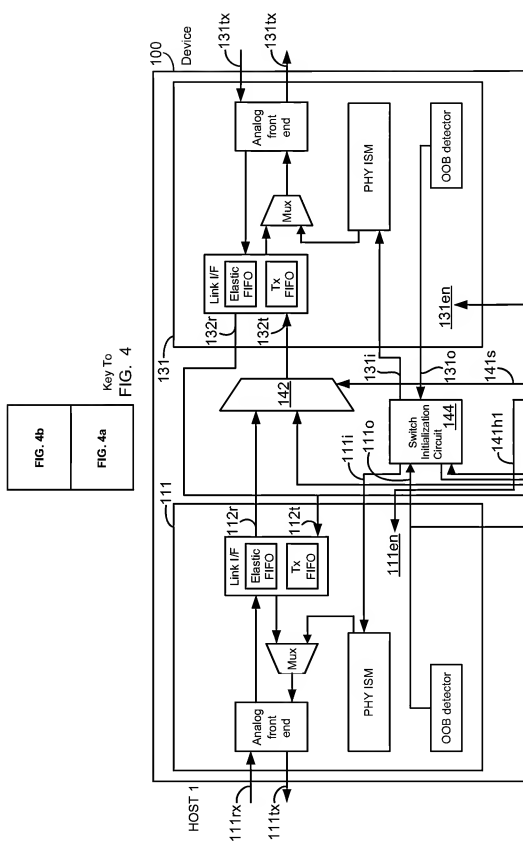
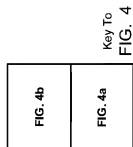


FIG. 4a



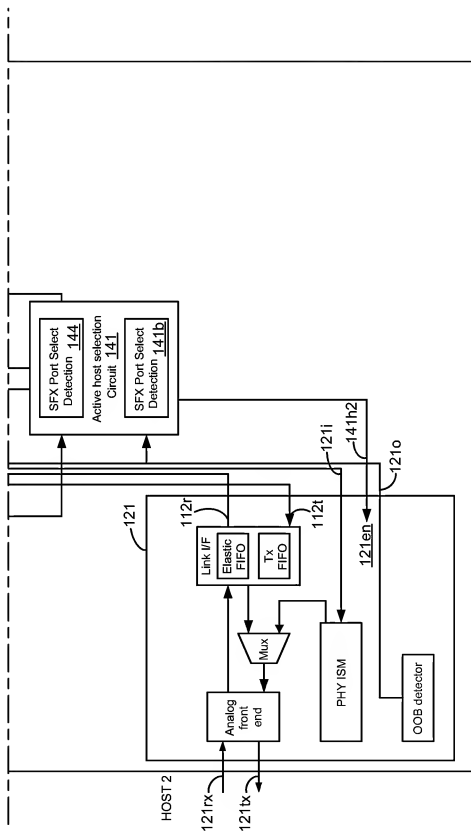


FIG. 4b

FIG. 5a	FIG. 5b
FIG. 5c	Key To FIG. 5

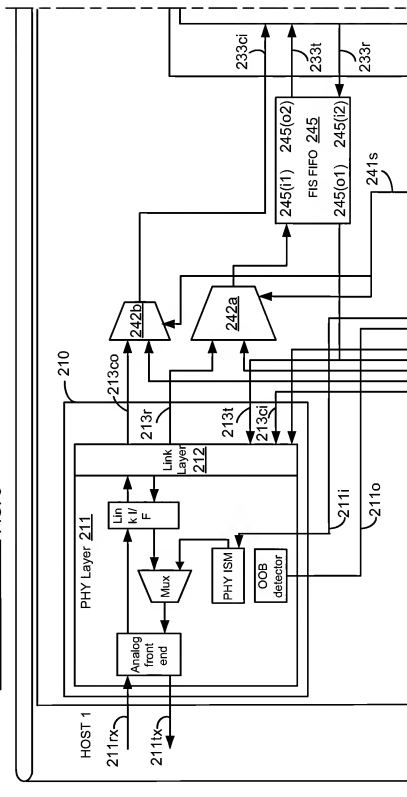


FIG. 5a

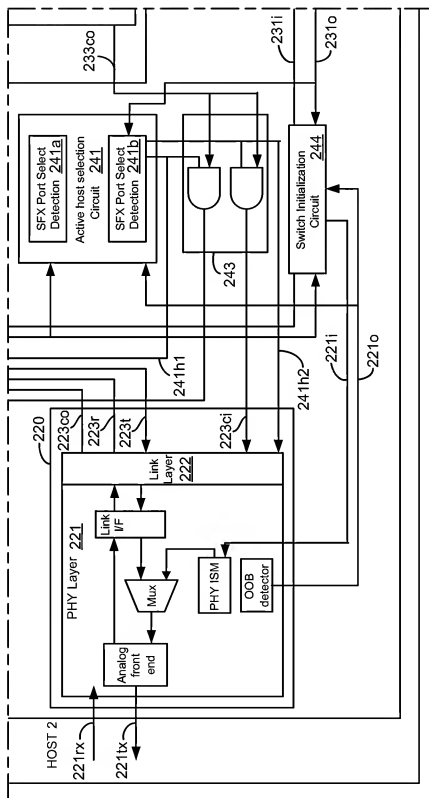


FIG. 5c

FIG. 6a

Key To

FIG. 6

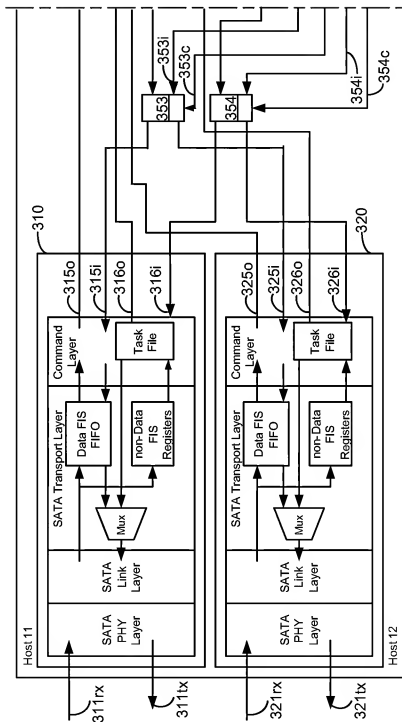


FIG. 6a

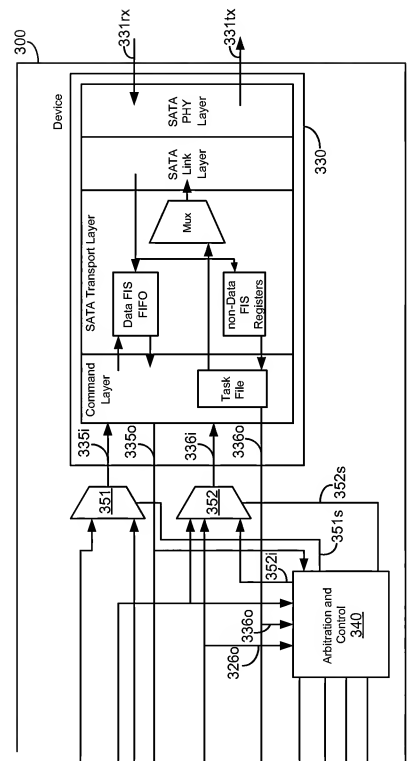


FIG. 6b

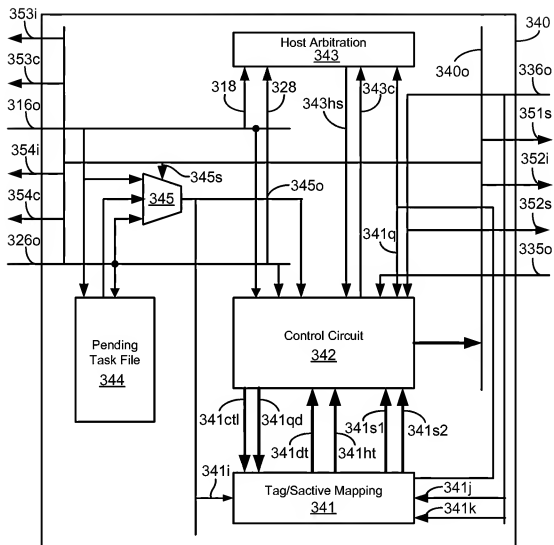


FIG. 7a

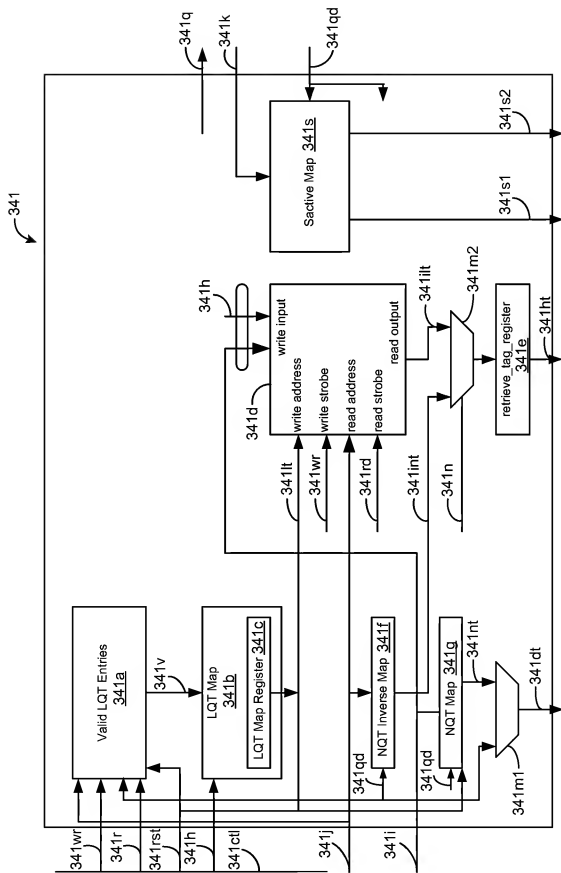


FIG. 7b

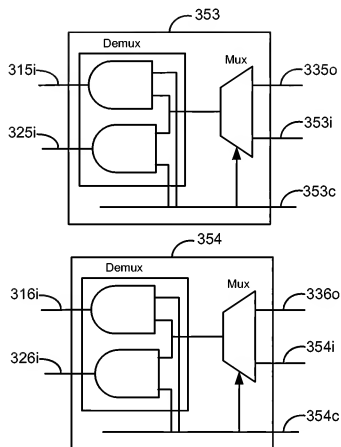


FIG. 7c

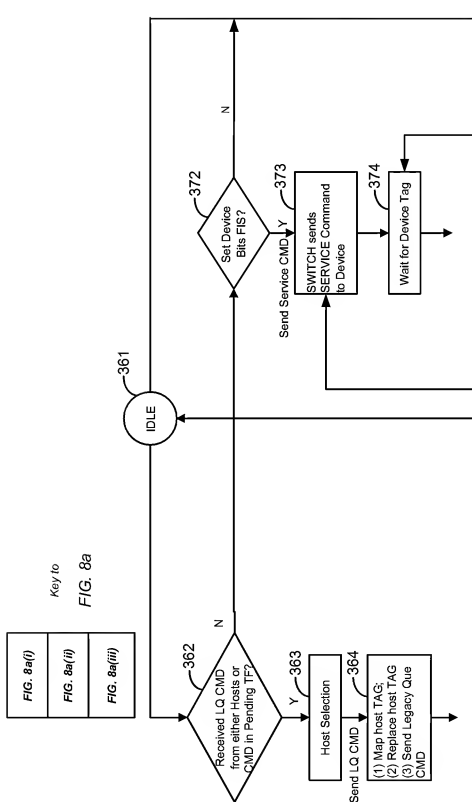


FIG. 8a(i)

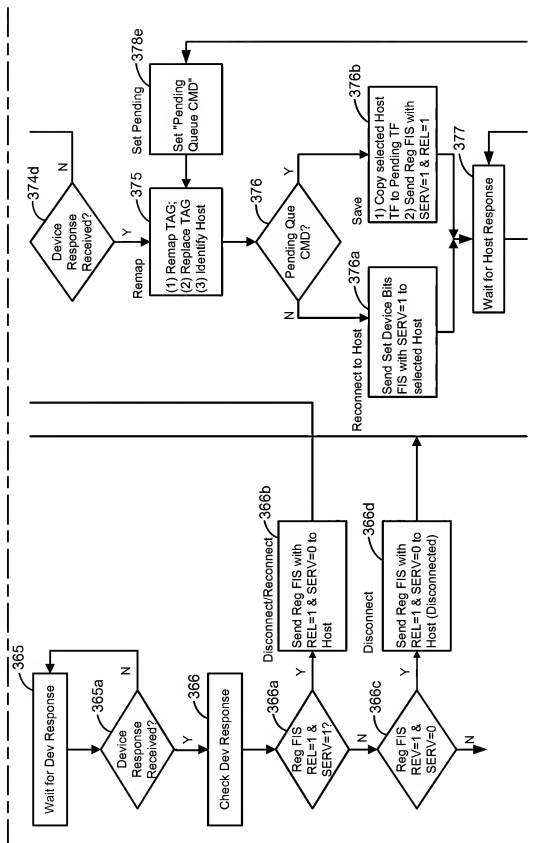


FIG. 8a(ii)

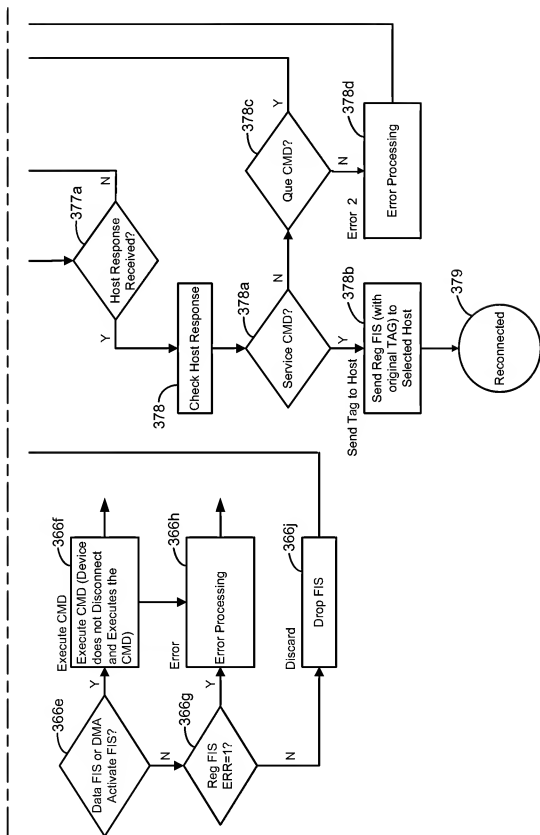


FIG. 8a(iii)

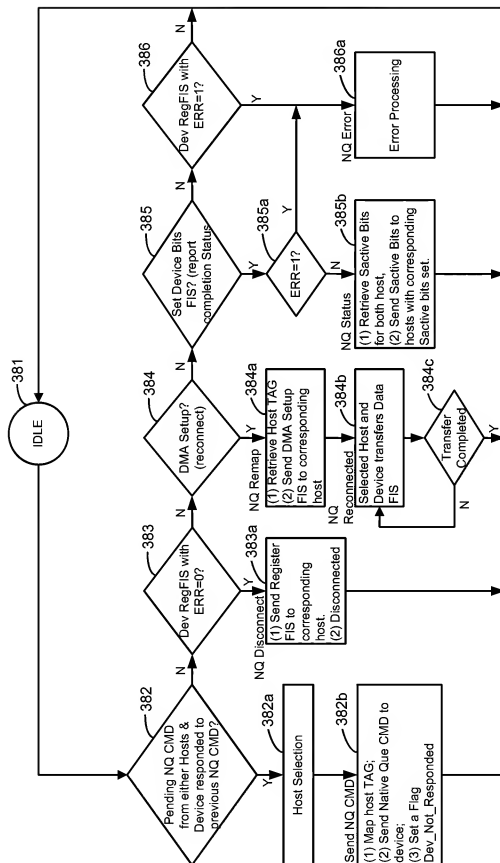


FIG. 8b

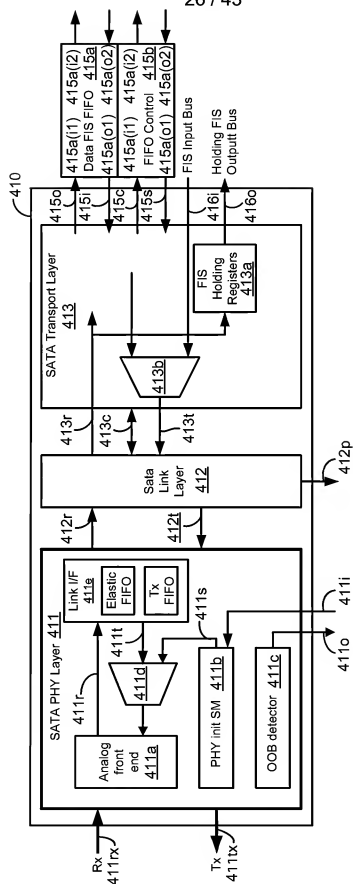


FIG. 9

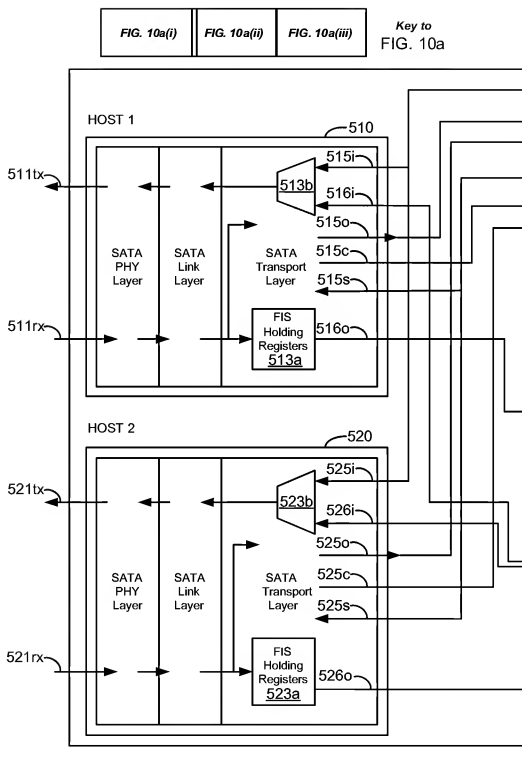


FIG. 10a(i)

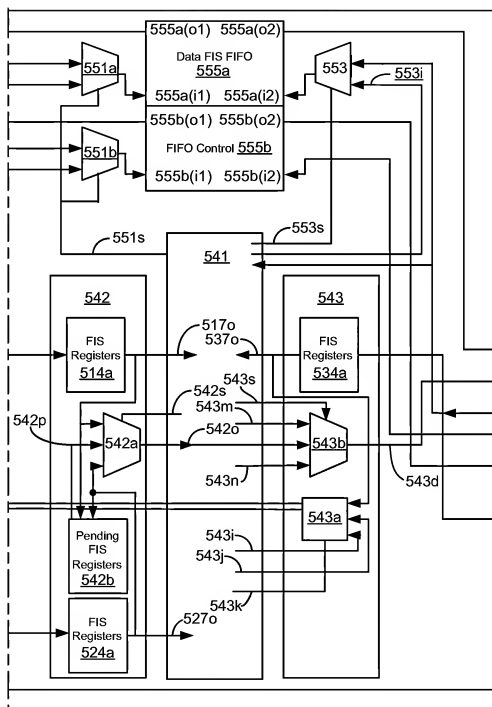


FIG. 10a(ii)

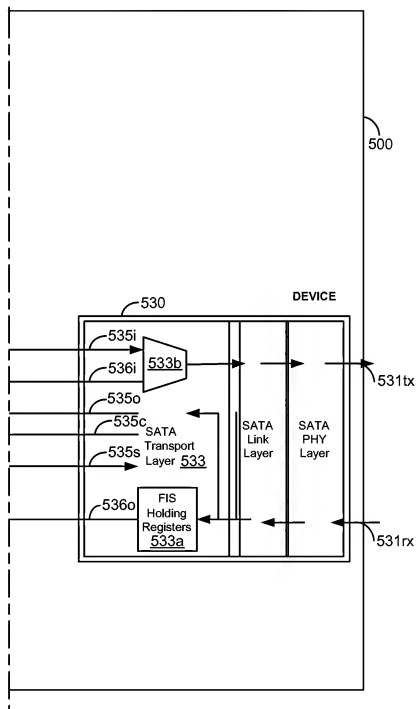
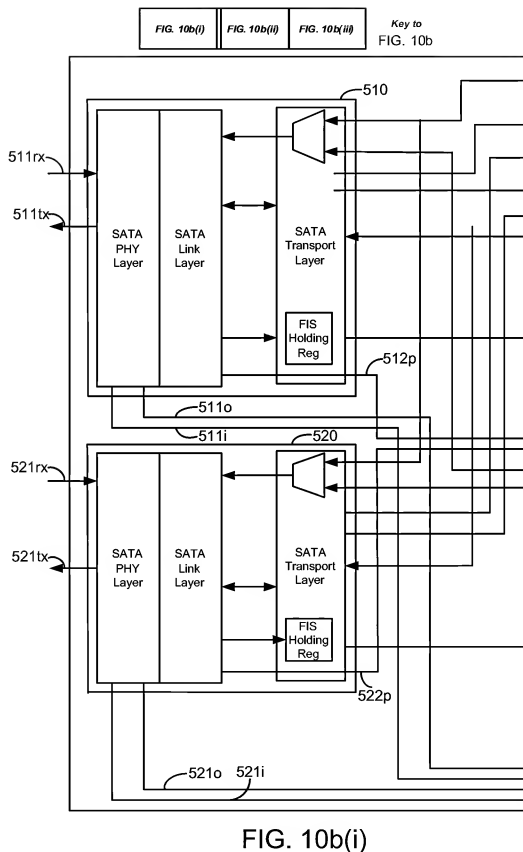


FIG. 10a(iii)



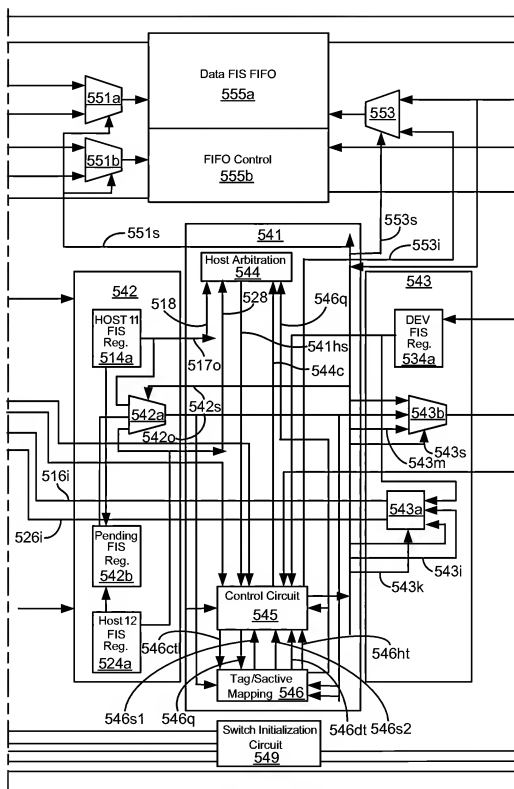


FIG. 10b(ii)

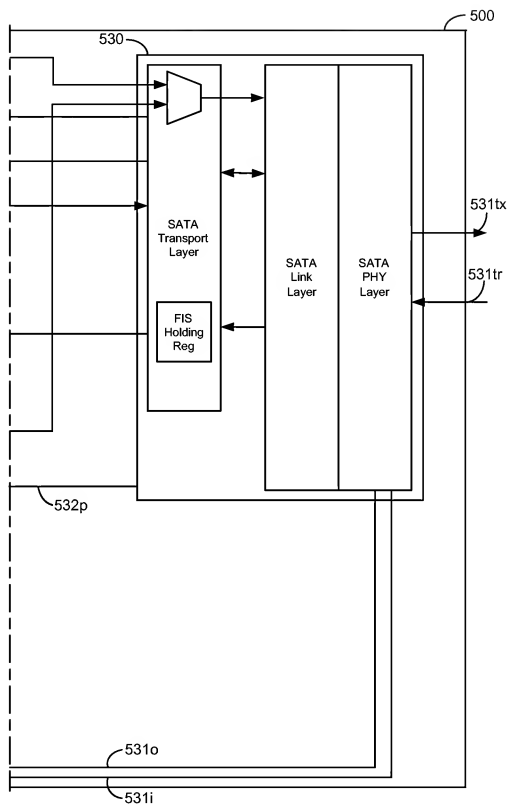


FIG.10b(iii)

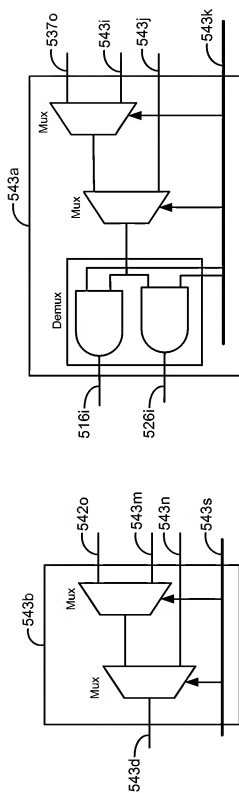
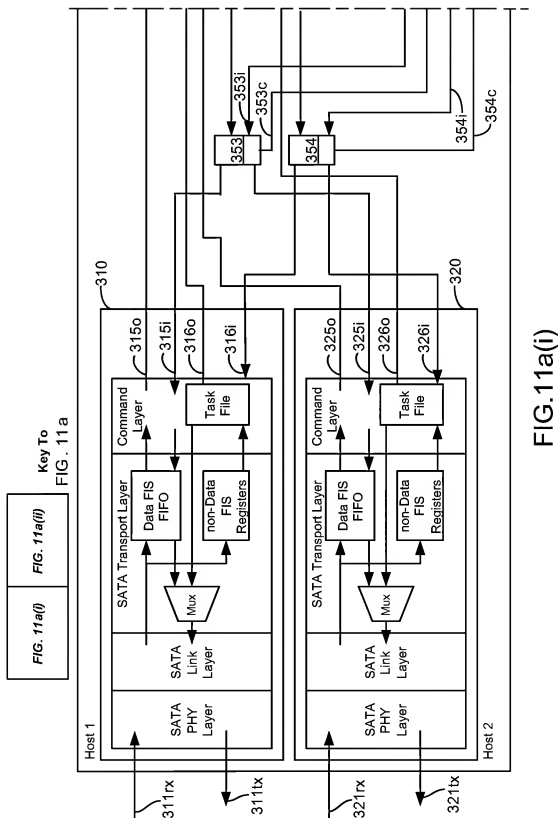


FIG.10c



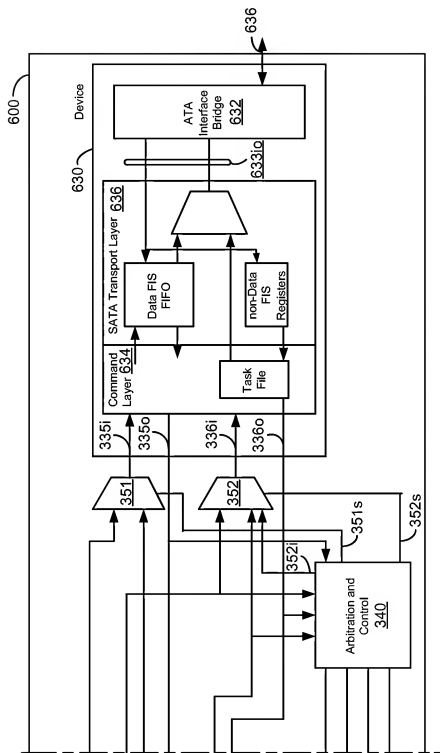
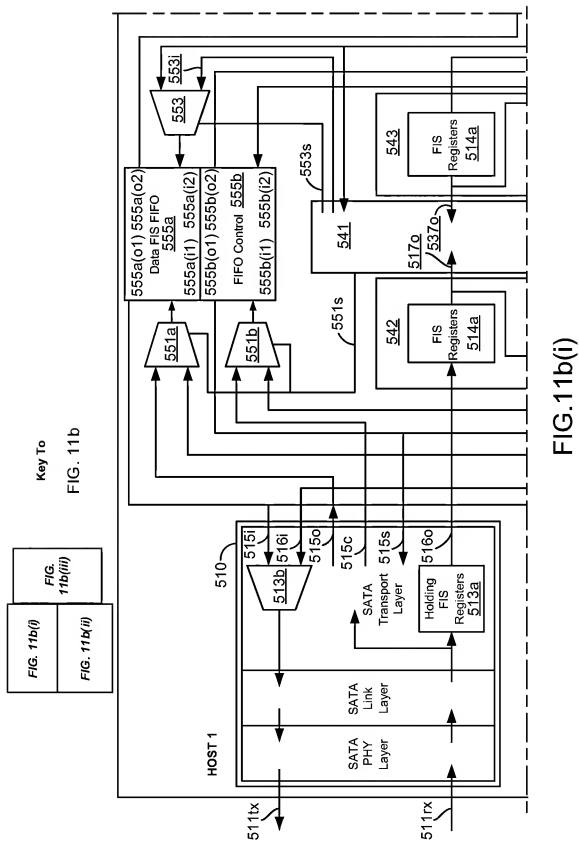
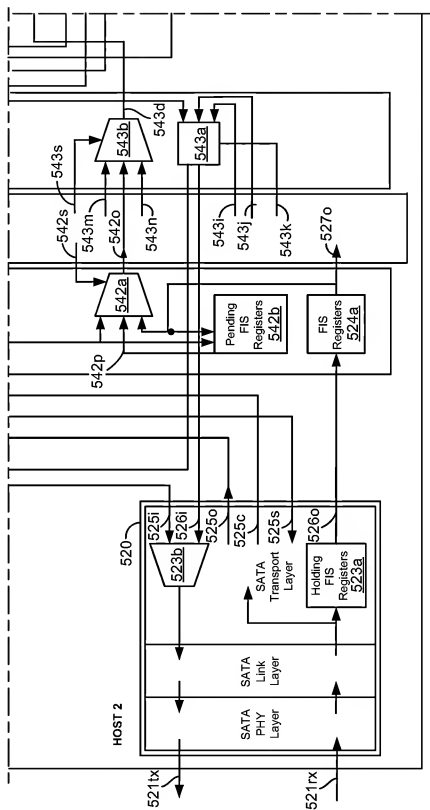


FIG.11a(ii)





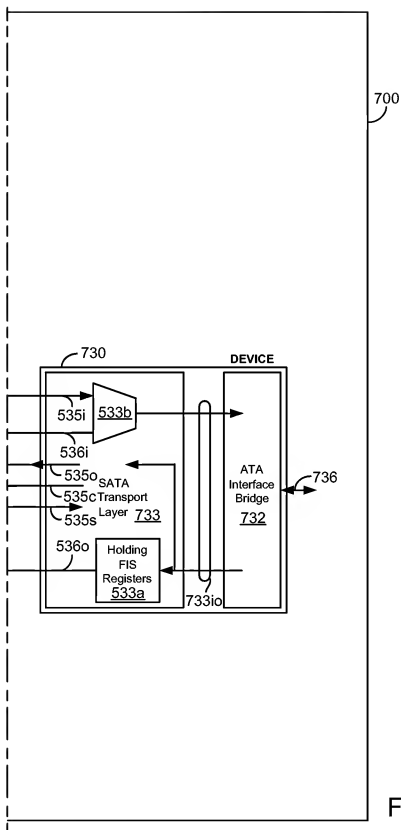


FIG.11b(iii)

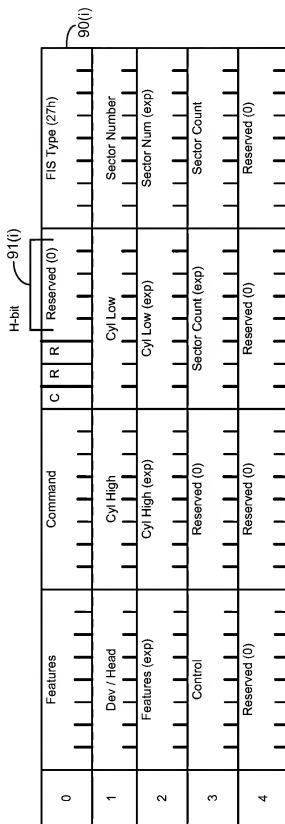


FIG. 12(i) Register FIS Host to Device

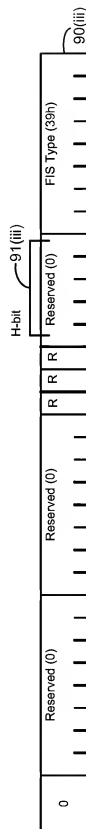


FIG. 12(iii) DMA Activate FIS, Device to Host

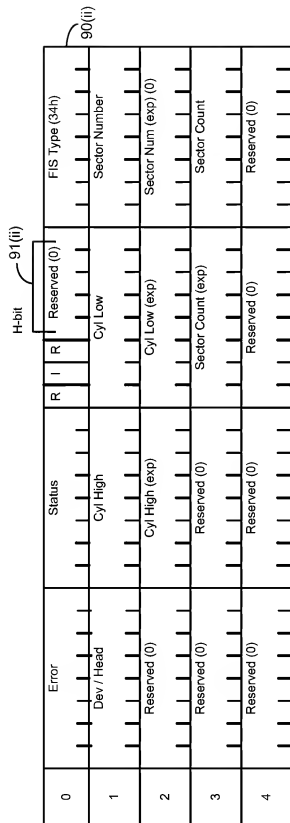


FIG. 12(ii) Register FIS Device to Host

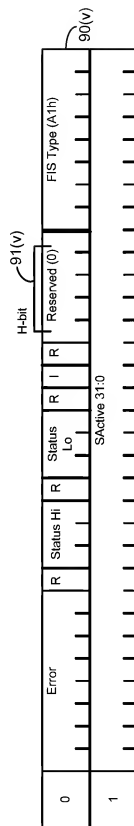


FIG. 12(v) Set Device Bits FIS

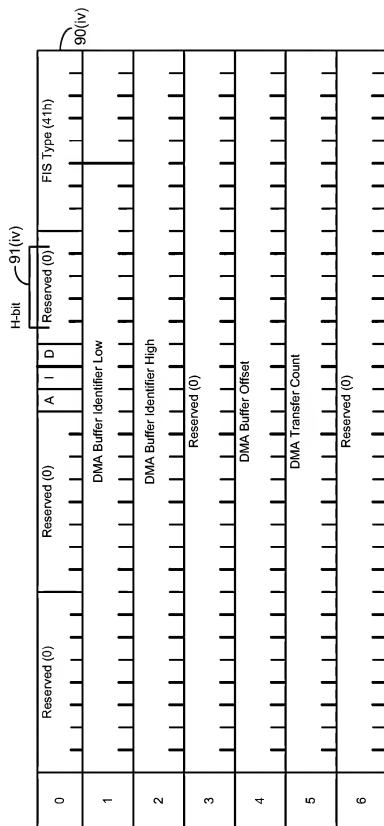


FIG. 12(iv) DMA Setup FIS

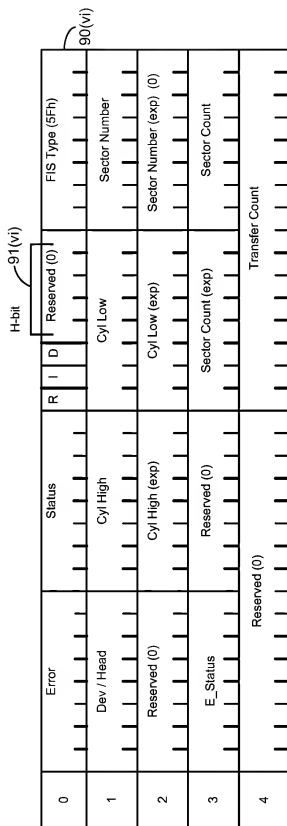


FIG. 12(vi) PIO Setup FIS

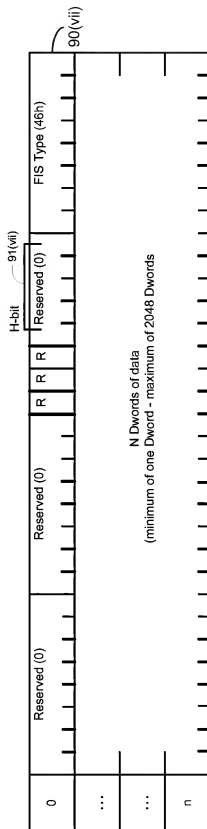


FIG. 12(vii) Data FIS

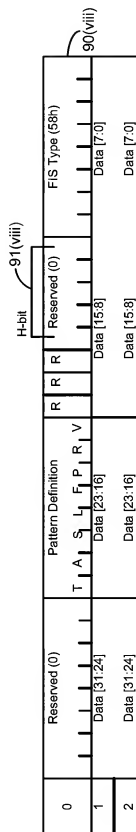


FIG. 12(viii)BIST Activate FIS